ABSTRACT

A programmable logic device includes a gate array formed from programmable logic elements, and at least one address decoder structure. The address decoder has a first stage, for receiving bits of an address, and for masking out a first group of least significant bits of said address; a second stage, for comparing a second group of most significant bits of said address with respective comparison bits; and a third stage, for providing an output when all of the bits in said second group of bits of said address match their respective comparison bits. Thus, the address decoder can determine when a received address falls within a range of addresses associated with the address decoder. Multiple address decoders may be provided at spaced apart locations within the gate array, and one address decoder can be associated with each slave device implemented in the gate array. The programmable logic device may be used to implement a bus structure, with a bus master which may be in the form of an embedded processor. One of the multiple address decoders can then be associated with each slave device in the bus structure.